In re application of	:	Trivedi et al.
Appl. No.	:	10/038,305
Filed	:	January 2, 2002
For	:	METHOD OF FORMING A DUAL DAMASCENE INTERCONNECT BY SELECTIVE METAL DEPOSITION
Examiner	:	Thanh T. Nguyen
Art Unit	:	2813

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September 15, 2004
(Date)

Sanjivpal S. Gill
Sanjivpal S. Gill, Reg. No. 42,578

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate is an Appellants' Brief to the Board of Patent Appeals:

(X) Fee for filing brief in the amount of $330 is enclosed.

(X) A check in the amount of $330 to cover the foregoing fees is enclosed.

(X) If applicant has not requested a sufficient extension of time and/or has not paid any other fee in a sufficient amount to prevent the abandonment of this application, please consider this as a Request for an Extension for the required time period and/or authorization to charge our Deposit Account No. 11-1410 for any fee which may be due. Please credit any overpayment to Deposit Account No. 11-1410.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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9/15/04
(Date)

Sanjivpal S. Gill
Sanjivpal S. Gill, Reg. No. 42,578

ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANT'S BRIEF

Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief relates to an appeal to the Board of Patent Appeals and Interferences of the final rejection set forth in an Office Action mailed April 19, 2004 in the above-captioned application.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

The above-captioned application was originally filed with Claims 1-23. In the course of prosecution, Claims 1 and 11-16 were cancelled. Claims 2-10 and 17-23 are thus pending in the present application, and were finally rejected in the Office Action dated April 19, 2004. The final rejection was affirmed in an Advisory Action dated July 12, 2003.

Accordingly, Claims 2-10 and 17-23 are the subject of this appeal. These claims are attached hereto as Appendix A.

IV. STATUS OF AMENDMENTS

The claims before the Board appear as they were finally rejected. As noted above, these pending claims are attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

The claimed invention relates generally to forming integrated circuits and, more particularly, to forming vertically-extending electrical contacts in insulating material by filling openings in the insulating material with different metals.

Due to a continuing demand for faster and smaller electronics, the sizes of integrated circuits are constantly being decreased. Integrated circuits typically comprise numerous electrical devices, which can be located at different vertical levels and separated by insulating material. Electrical devices on different levels are typically electrically connected by metal contacts that fill openings, or contact vias, in the insulating material. Because of electrical and practical constraints, the widths of the contact vias are decreasing at a faster rate than their depths, continually leading to increases in the aspect ratios of the contact vias. *See* the Specification, p. 2.

Aluminum is commonly used to form conductive interconnects due to its relatively high conductivity. Aluminum can be deposited by physical vapor deposition (PVD), *e.g.*, sputtering. As aspect ratios have increased, however, PVD of aluminum has been found to be inadequate for filling vias. In particular, PVD of aluminum may not completely fill the vias, causing various physical and electrical problems. *See* the Specification, p. 2.

In contrast, some less conductive metals, such as tungsten, can be more completely deposited into vias because processes which allow more complete fill of vias are available for

these metals. A significant drawback of these metals, especially for higher aspect ratio vias, however, is their low conductivity compared to aluminum. As a result, filling of vias using, *e.g.*, chemical vapor deposition (CVD) of tungsten, and the formation of high conductivity contacts in the vias have been conflicting goals. *See* the Specification, p. 2.

The present invention overcomes the above-described problems by providing a method of adequately filling vias 25 while also forming contacts with good conductivity. Because it can be difficult to completely fill a via 25 with a high conductivity metal such as aluminum, the aspect ratio of the via 25 is effectively decreased by first partially filling the via 25 with a less conductive metal 55, such as tungsten, which is easier to deposit into the via 25. Thus, the floor of the via 25 is raised, effectively decreasing the aspect ratio of the via 25 for subsequent depositions and allowing a higher conductivity metal 60 to be more easily deposited into the via 25. *See, e.g.,* the Specification, p. 11.

In addition, while the desire for a high conductivity contact has indicated the use of high conductivity metals such as aluminum for forming the entire contact in a via 25, Appellants have found that filling about one-third to two-thirds of the height of the via 25 with a relatively low conductivity metal 55 is sufficient to effectively reduce the aspect ratio of the via 25 and thus facilitate deposition of a higher conductivity metal 60, without significantly decreasing the conductivity of the contact due to use of the less conductive metal 55. *See, e.g.,* the Specification, p. 8.

Accordingly, both independent Claims 6 and 17 recite filling between one-thirds to two-thirds of the height of a contact via with a first, relatively low conductivity metal and then filling a remainder of the via with a second, relatively high conductivity metal.

VI. ISSUES BEFORE THE BOARD

There are two issues before the Board in this appeal:

A. Whether Claims 2-10 and 17-23 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann (U.S. Pat. No. 6,156,651) in view of various secondary references.

B. Whether Appellants have established the criticality of the recited deposition levels of the less conductive metal.

VII. GROUPING OF CLAIMS

For purposes of the present appeal, Claims 2-10 and 17-23, each reciting filling a first metal to a height of between one-third and two-thirds of the height of a contact via and filling a remainder of the contact via with a second metal that is more conductive than the first metal, stand and fall together. Appellants reserve the right, however, to separately argue, in subsequent continuing applications, the patentability of various dependent features not addressed herein.

VIII. APPELLANTS' ARGUMENT

In the final Office Action mailed April 19, 2004, the Examiner rejected Claims 2-9 and 17-20 as being unpatentable under 35 U.S.C. § 103(a) over Havemann (U.S. Patent No. 6,156,651) in view of Liu (U.S. Patent No. 6,211,085). Claims 21-23 were rejected as being unpatentable under 35 U.S.C. § 103(a) over Havemann in view of Omura (U.S. Patent No. 6,028,362). Dependent Claim 10 was rejected as being unpatentable under 35 U.S.C. § 103(a) over Havemann in view of Yu *et al.* (U.S. Patent No. 6,365,514). Thus, each rejection is based upon the asserted teachings of Havemann.

Appellants submit that Havemann does not teach all that has been asserted and that the art of record, individually or in combination, fail to teach or suggest the combination of features recited in independent Claims 6 and 17.

Havemann teaches a method for forming conductors in vias and trenches. Havemann states that a metal is first selectively deposited into part of the via by electrodeposition and then the via and trench are filled using another deposition process. For example, Havemann discloses:

> FIG. 6C shows the structure after deposition of selective metal (e.g., ***aluminum***) here with the selective metal deposition initiated by a conductive area in the substrate at the bottom of the via. In FIG. 6E conductor metal 70 has been deposited over the entire area, including filling the conductor grooves (e.g., PVD or CVD ***aluminum***).

Havemann, Col. 6, lines 39-46 (emphasis added). Havemann notes that the "selective deposition fills the via to less than the height of the [via]." *Id.* at Col. 5, lines 54-56. Havemann discloses that elective deposition can be accomplished by electrochemical deposition, *e.g.*, electroplating by using a conductive seed layer to initiate metal deposition. *See, e.g., id.* at Col. 2, lines 25-29; Col. 3, line 66 to Col. 4, line 16; and Col. 6, line 40-43.

In addition, Havemann states that the "conductors and vias of this invention will generally be either copper, tungsten or aluminum or combinations thereof." *Id.* at Col. 3, lines 18-20. In its claims, Havemann clarifies that the term "combinations thereof" refers to a ***mixture*** of metals that form a single conductor, rather than pure metals that are separately deposited. For example, Claim 1 of Havemann recites "depositing a first conductor metal" and dependent Claims 4, 12 and 20 of Havemann each clarify that "said conductor metal consists of essentially aluminum, tungsten, copper or combinations thereof." Thus, Havemann only teaches examples of deposition in which the ***same*** metal is deposited over itself.

Citing these teachings, the Examiner has asserted that Havemann teaches selective deposition of tungsten into a via, to between about one-third and two-thirds of the height of the via, followed by aluminum deposition. In particular, the Examiner has asserted that Havemann teaches:

> depositing a first metal (tungsten, 66, see col. 3, lines 19-21) (as claimed in claims 2, 15 and 19) ... to partially fill the contact via (see figure 6C), and filling a remainder of the contact via with a second metal (70, aluminum, see figure 6E, as claimed in claims 2 and 20) ... the second metal of aluminum being more conductive than the first metal of tungsten ... wherein depositing the first metal comprises filling the contact via to a height between about one-third and two thirds of height [sic] of the contact via (see figure 6C, col. 5, lines 39-41, 54-61).

Office Action mailed April 19, 2004. In the Advisory Action mailed July 12, 2004, the Examiner elaborated on her rationale for the rejections and stated that Havemann teaches:

> filling the opening less than the height of the dielectric layer which interpretate [sic; is interpreted as] as anywhere less than completely fill [sic; filling the via] ... the piro reference that discloseds a reange [sic; prior art reference that discloses a range] encompassing a somewhat narrower claimed range is sufficient to establish a prima facie case of obviousness. therefore [sic], the burden is shifted to the applicant to show [a] side by side example of [sic; that the] overlapping range as taught by Havemanni [sic; Havemann] does not teach the unexpected result as the present invention teaches ... [In addition] it is obvious that the first layer is tungsten and the second is aluminum because the process would raise [the] contact floor [and] allows [a] more conductive metal to be deposited by [a] less conformal deposition.

A. <u>The Examiner has misinterpreted Havemann; Havemann does not teach selectively depositing a relatively low conductivity metal and then depositing a relatively high conductivity metal into a contact via.</u>

The claims on appeal recite a particular deposition sequence. In particular, independent Claims 6 and 17 each recite selectively depositing a first metal (*e.g.*, tungsten) and then depositing a second metal (*e.g.*, aluminum) that is more conductive than the first metal. Thus, to establish a *prima facie* case of obviousness, the Examiner must show that the art of record teaches or suggests this particular sequence of metal depositions. *See, e.g., In re Rouffet*, 47 U.S.P.Q.2d 1453, 149 F.3d 1350 (Fed. Cir. 1998). As noted above, the Examiner has relied upon Havemann for teaching tungsten deposition followed by aluminum deposition.

Applicants do not argue here that Havemann does not teach that tungsten and aluminum can individually be deposited into the structures taught by that reference at some point. Havemann, however, does not teach the ***combination*** of first tungsten and then aluminum deposition asserted by the Examiner; rather, Havemann fails to teach any particular combination of deposition of a relatively low conductivity metal followed by deposition of a relatively high conductivity metal.

The Examiner has pointed to Figure 6 of Havemann as supporting the assertion that a combination of tungsten deposition followed by aluminum deposition is taught. This is incorrect. Havemann discusses Figure 6 at column 6, lines 40-46 and clearly states, as noted above, that Figure 6 shows a two-step deposition of metal over metal. Havemann does not teach that these metals should have different conductivities, however; rather, Havemann only gives the example of depositing the same metal, ***aluminum***, in a two-step deposition. Moreover, column 3, lines 19-21, which is also relied upon by the Examiner, is inapposite; while column 3, lines 19-21 does state that tungsten may be part of the deposition process, that text does not state that the metal deposited ***in*** the via of Figure 6 and prior to aluminum deposition is tungsten.

The Examiner's reliance on claims 2, 15, 19 and 20 of Havemann is similarly misplaced. Claims 2, 15 and 19 of Havemann concern various types of processing (*e.g.*, sputtering, chemical mechanical polishing), but do not disclose the identity of the metal filling the via. Moreover, as discussed above, Claim 20 actually clarifies that the phrase "combinations thereof" refers to the fact that the deposited metal can be a single mixture of metals, not that different metals are deposited one over the other.

The Examiner appears to have recognized these deficiencies and has stated, in the Advisory Action, that tungsten deposition followed by aluminum deposition is obvious to raise the contact floor to allow the more conductive metal to be deposited by a less conformal deposition. Thus, the Examiner appears to have provided this rationale as a suggestion to combine tungsten deposition into a via with aluminum deposition, with the tungsten deposition occurring before the aluminum deposition. As noted above, Appellants do not argue here that tungsten and aluminum are not separately listed in Havemann. To establish a *prima facie* case of obviousness, however, the Examiner must establish that the prior art both suggests the sequence of relatively low conductivity metal (*e.g.*, tungsten) deposition followed by relatively high conductivity metal (*e.g.*, aluminum) deposition and that the prior art provides a reasonable expectation of success. *In re Dow Chemical Co.*, 5 U.S.P.Q.2d 1529, 837 F.2d 469 (Fed. Cir. 1988) ("Both the suggestion [to combine] and the expectation of success, must be founded in the prior art, not in the applicant's disclosure.").

Initially, Appellants note that nowhere does Havemann or the other art of record provide the Examiner's stated rationale for selecting the metal combination of tungsten followed by aluminum. Rather, it is ***Appellants*** that have disclosed a scheme for damascene processing based upon the principles of raising the via floor with a less conductive metal and filling the remainder of the via with a more conductive metal. In view of the silence of the art of record, it is impermissible for the Examiner to reconstruct Appellants' invention based upon the hindsight gained from Appellants' Application. Instead, the "examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998); *see also In re Gorman*, 18 U.S.P.Q.2d 1885, 1888 (Fed. Cir. 1991) ("It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps."). In this case the Examiner has not provided any rationale from the prior art for depositing a relatively low conductivity metal followed by a relatively high conductivity metal.

In addition, Appellants submit that the skilled artisan would understand that Havemann does not suggest depositing a less conductive metal such as tungsten followed by a more conductive metal such as aluminum. Appellants note that, in addition to not providing a rationale for tungsten

deposition before aluminum deposition, Havemann does not provide any examples of the deposition of two different metals, one over the other. For example, as discussed above, Havemann in its Figure 6 only provides an example of a two-step deposition process using the same metal, namely aluminum.

Moreover, as also noted above, Havemann teaches that the earlier metal deposited into the via illustrated in Figure 6 is electrochemically deposited using a conductive seed layer. *See*, Col. 6, lines 42-43 ("the selective metal deposition [is] initiated by a conductive area in the substrate at the bottom of the via."). Appellants note that it is well-known to the skilled artisan that tungsten cannot be successfully electrochemically deposited to form contacts in vias. This is evident, for example, in the article "Processing and Integration of Copper Interconnects," in which Jackson *et al.* state that electroplating is available for copper but not for tungsten or for aluminum. *See*, Jackson *et al.*, Solid State Technology, March 1998, p. 3 (noting that "electroplating is an attractive alternative deposition method for copper that is not available for tungsten or aluminum). In fact, tungsten can be used to "poison" seed layers to prevent electroplating in some circumstances. *See, e.g.*, U.S. Patent No. 6,605,534 (stating, at Col. 5, lines 2-10, that "tungsten is an electroplating contaminant which effectively retards or prevents electroplating"). In addition, while Havemann teaches that electroplating is used for deposition into vias, it does not provide any teachings extending the capabilities of the skilled artisan to electroplate every single one of the listed metals of aluminum, tungsten and copper. Thus, given the known limitations of electroplating, Appellants submit that the skilled artisan would not read Havemann as suggesting first depositing tungsten and then aluminum nor would the skilled artisan have expected that tungsten could be successfully selectively deposited into the via illustrated in Figure 6 of Havemann, as asserted by the Examiner.

As a result, Appellants submit that the Examiner has not shown that Havemann teaches or suggests the asserted sequence of selectively depositing a relatively low conductivity metal followed by depositing a relatively high conductivity metal into a contact via. Appellants also submit that the other art of record does not satisfy this deficiency. Rather, Appellants submit that such a suggestion is not present in the prior art because the skilled artisan would not have expected the asserted deposition of tungsten in Havemann's process to be successful.

Accordingly, in view of the clear deficiencies of the art of record, especially Havemann, Appellants submit that the Examiner has failed to establish a *prima facie* case of obviousness

with respect to independent Claims 6 and 17. Consequently, Appellants submit that Claims 6 and 17, and Claims 2-5, 7-10, and 18-23, depending from Claims 6 or 17, are allowable over the art of record.

B. Appellants have shown the criticality of depositing a relatively low conductivity metal to between one-third and two-thirds of the height of a contact via and then filling the contact via with the a relatively high conductivity metal.

Assuming *arguendo*, that the Examiner has established a *prima facie* case of obviousness, Appellants submit that the pending claims are allowable because Appellants have established the criticality of the recited deposition levels. *See, e.g., In re Antonie*, 559 F.2d 618, 195 U.S.P.Q. 6 (C.C.P.A 1977) and *In re Rijckaert*, 9 F.3d 1531, 28 U.S.P.Q.2d 1955 (Fed. Cir. 1993) (finding that claims reciting a particular numerical limitation or relationships were non-obvious due to the recognition of the criticality of that numerical limitation or relationship). In particular, the Specification clearly discloses the criticality of depositing the less conductive metal to between one-third and two-thirds of the height of a contact via.

The recited deposition levels represent a resolution of two competing goals: the raising of the via floor as high as possible to facilitate deposition of the more conductive metal and the desire to form a contact with as high conductivity as possible. Appellants have recognized that certain relatively low conductivity metals can be readily selectively deposited into contact vias, whereas relatively high conductivity metals can be more difficult to deposit selectively. Thus, Appellants have devised a scheme whereby the requirements for deposition are eased by raising the floor of the via to effectively decrease the aspect ratio of the via. At the same time, Appellants have ensured that the resulting structure has good overall conductivity. *See, e.g.,* the Specification, p. 11. In particular, these conflicting goals have been resolved by depositing the less conductive metal to "between about one-thirds and two-thirds" of the height of the contact via. *See, e.g.,* the Specification, p. 8. Appellants submit that the art of record does not recognize the ability to resolve the above-noted conflicting goals by the recited process.

Accordingly, in view of the established criticality of the recited deposition levels, Appellants submit that independent Claims 6 and 17 are allowable over the art of record. Because Claims 2-5, 7-10, and 18-23, depend from Claims 6 or 17, Appellants submit that these claims are also allowable over the art of record.

C. Conclusion

The Examiner has not met his burden for establishing a *prima facie* case of obviousness. The art of record, and Havemann in particular, fail to teach or suggest selective deposition of a relatively low conductivity metal followed by deposition of a relatively high conductivity metal. Moreover, given the limitations of electroplating known to the skilled artisan, the art of record does not suggest depositing a less conductive metal such a tungsten followed by depositing a more conductive metal such as aluminum into the via disclosed by Havemann, nor does the art of record provide a reasonable expectation that this deposition sequence would be successful in combination with Havemann.

Moreover, even if a *prima facie* case of obviousness were established, Appellants submit that the criticality of the recited deposition levels has been established.

Accordingly, Appellants submit that the rejections of Claims 2-10 and 17-23 are improper and that these claims are allowable over the art of record.

IX. APPENDIX A

Attached hereto is a copy of the finally rejected claims in the present case that are the subject of this appeal.

X. APPENDIX B

Attached hereto is a copy of Havemann (U.S. Patent No. 6,156,651), the primary reference cited by the Examiner in all rejections.

XI. APPENDIX C

Attached hereto are copies of Jackson *et al.*, Solid State Technology, March 1998 and U.S. Patent No. 6,605,534 to Chung *et al.*, discussing electroplating using tungsten and/or aluminum.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 9/15/04

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APPENDIX A

Finally Rejected Claims on Appeal

1. (Cancelled).

2. (Previously Presented) The method of Claim 6, wherein the first metal comprises tungsten and the second metal comprises aluminum.

3. (Previously Presented) The method of Claim 6, wherein depositing comprises a selective chemical vapor deposition.

4. (Original) The method of Claim 3, wherein depositing comprises depositing a ratio of first metal thickness over the conductive element to first metal thickness over insulating surfaces of the dual damascene structure of greater than about 10:1.

5. (Previously Presented) The method of Claim 6, wherein filling comprises flowing aluminum at a temperature between about 400°C and 550°C.

6. (Previously Presented) A method of forming an integrated circuit, comprising:

forming a dual damascene structure in insulating material over a semiconductor substrate, the dual damascene structure comprising a trench and a contact via extending from a bottom of the trench to expose a conductive element;

depositing a first metal selectively over the conductive element relative to insulating surfaces of the dual damascene structure to partially fill the contact via; and

filling a remainder of the contact via with a second metal, the second metal being more conductive than the first metal,

wherein depositing the first metal comprises filling the contact via to a height between about one-third and two-thirds of a height of the contact via.

7. (Previously Presented) The method of Claim 6, wherein depositing the first metal comprises filling the contact via to a height between about one-half and two-thirds of a height of the contact via.

8. (Previously Presented) The method of Claim 6, wherein filling comprises overflowing the contact via to at least partially fill the trench with the second metal.

9. (Original) The method of Claim 8, wherein filling comprises a hot aluminum deposition.

10. (Original) The method of Claim 9, further comprising following the hot aluminum deposition with a cold aluminum deposition.

11-16. (Cancelled).

17. (Previously Presented) A method for forming an integrated contact plug, comprising:

forming a dual damascene contact via in insulating material, wherein the dual damascene contact via has a height extending from a conductive element at a bottom of the contact via to a bottom of a dual damascene trench directly over the contact via;

depositing a first metal to fill between about one-thirds and two-thirds of the height of the contact via; and

filling a remainder of the contact via with a second metal, wherein the second metal is more conductive than the first metal and partially fills the trench.

18. (Original) The method of Claim 17, wherein depositing comprises filling the contact via to between about one-half and two-thirds of the height of the contact via.

19. (Original) The method of Claim 17, wherein the first metal comprises tungsten.

20. (Original) The method of Claim 17, wherein the second metal comprises aluminum.

21. (Original) The method of Claim 17, wherein the contact via and the trench are lined with a barrier layer before depositing the first metal.

22. (Original) The method of Claim 21, wherein the barrier layer comprises a metal nitride.

23. (Original) The method of Claim 17, wherein the contact via and the trench are lined with an adhesion layer before depositing the first metal.

Processing and integration of copper interconnects

Processing and integration of copper interconnects

Robert L. Jackson, Eliot Broadbent, Theodore Cacouris, Alain Harrus, Maximillian Biberger, Evan Patton, Tom Walsh, Novellus Systems, San Jose, California

The conversion from aluminum to copper interconnects introduces many new processes and materials into semiconductor manufacturing, including damascene process flows and electroplating unit processes. Chemical vapor deposition (CVD) for complete copper fill may return to replace electroplating in future device generations. Many integration problems involve the thin-films that function as diffusion barriers and seed/wetting layers.

The transition from aluminum to copper interconnects in semiconductor manufacturing is rapidly accelerating, as evidenced by recent press announcements from major microprocessor companies. Two primary factors drive this transition - the lower resistivity and the increased electromigration resistance that copper offers relative to aluminum.

Both of these factors address major problems faced by microprocessor manufacturers. Beyond the 0.35-?m device generation, interconnect RC (i.e., the product of the metal resistance and the dielectric capacitance) delays significantly limit microprocessor clock speed. Recent reports [1, 2, 3] show that much of this limitation can be overcome by switching from an aluminum to a copper primary conductor, without altering the dielectric.

The primary clock-speed advantage derived from the lower resistivity of copper is achieved by introducing copper at the upper interconnect levels, where conductor lengths can be of the same order as chip size. Beyond the 0.25-?m device generation, current densities in lower interconnect levels can induce electromigration failure of traditional doped-aluminum conductors. The increased electromigration resistance of copper helps overcome this limitation.

The general process flow for fabrication of copper interconnects is now reasonably well-established [4]. In the dual-damascene process (Fig. 1), via and line levels are fabricated concurrently, while in the single-damascene process, each level is fabricated separately. The dual-damascene process involves approximately 30% fewer steps than either the single-damascene process or the subtractive process currently used to fabricate aluminum interconnects [5]. As a result, dual-damascene processing should offer a significant cost advantage.

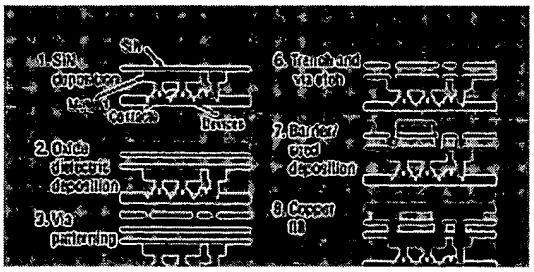


Figure 1. Dual-damascene process flow for fabrication of copper interconnects. This process flow shows the via-definition step followed by the trench-definition step.

Manufacturing implementation of the damascene process flow requires several new materials and processes, plus alterations to existing processes (Fig. 2). Two changes are particularly noteworthy. In the aluminum interconnect fabrication process, metal-etch is the critical step that defines the width and spacing of the interconnect lines, while the burden of planarizing each metal level is placed on the dielectric gap-fill and CMP steps. In the copper interconnect fabrication process, a simpler dielectric etch replaces metal-etch as the critical step that defines the width and spacing of the interconnect lines, while the burden of planarization shifts to the metal deposition and CMP steps. This article examines the primary manufacturing steps involved in fabricating copper interconnects, emphasizing the changes in materials and processes required to switch from aluminum to copper. We discuss the challenges expected for each step, as well as challenges that affect integration of the entire damascene process sequence.

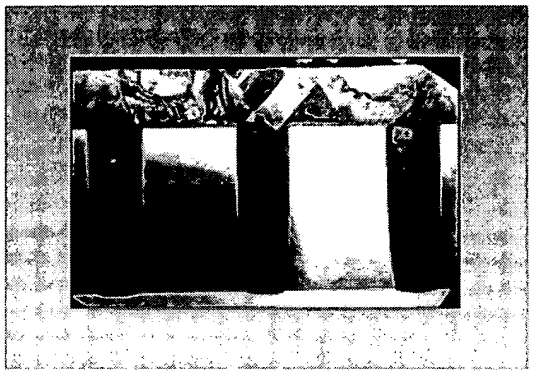


Figure 2. Summary of the major process technology changes required in the transition from the subtractive aluminum interconnect fabrication process to the copper damascene fabrication process.

557\MarchMarketing\Fig. 5

Dielectric deposition

The first step in the fabrication of each copper interconnect level is the deposition of a thin layer of silicon nitride. This layer serves as a barrier against the diffusion of copper between metal levels, and also as an etch-stop in the dielectric etch that defines the damascene vias. Because silicon nitride has a high dielectric constant, the nitride layer should be as thin as possible to avoid adding significantly to the interlevel capacitance of the complete dielectric stack. At the same time, the nitride layer must be low-stress, dense, and pinhole-free so that its diffusion barrier properties are not compromised. High-density is also critical to the nitride layer's performance as an etch-stop. This collection of properties may be better met by a nitride deposited using high-density plasma (HDP-CVD) methods, rather than by traditional PECVD.

Deposition of the primary silicon dioxide dielectric immediately follows deposition of the nitride etch-stop in the dual-damascene process flow. The nitride and oxide layers may be deposited sequentially in the same tool. A simple, undoped oxide deposited by PECVD will find widespread application as the primary dielectric in copper interconnects, since the gap-filling properties of HDP-CVD oxides will not be required. Fluorine-doped oxides can also be used to produce a lower dielectric constant material.

In the near future, low-k dielectrics will emerge as a replacement for silicon dioxide. Although the integration of copper with low-k dielectrics is not specifically addressed in this article, any process developed for copper interconnect fabrication should be compatible with the low-k dielectric materials that may be used in future generations.

Lithography

For each device generation, interconnect line and via dimensions are less demanding than the critical dimensions (CDs) found at the silicon level. As a result, lithographic patterning of single-damascene interconnects can take full advantage of established process flows used in front-end processing.

Dual-damascene processing, however, presents a tremendous challenge to lithographers. Trench structures must be created over topography (resulting from the previous via-etch step), presenting problems for the resist

coating, exposure, and development processes. Lithography problems may fundamentally limit use of the dual-damascene process beyond one or two additional device generations, particularly at the lower interconnect levels where the tightest CDs are encountered.

Via/trench etch

Via etch processes nearly identical to those required in damascene processing are already well-established. The same etch is currently used in the fabrication of tungsten plugs for both logic and memory devices. Trench-etch is a straightforward extension of the via etch process, except that much more material must be removed at the trench level.

The dual-damascene process sequence adds a new set of difficulties to the etch process. The primary problem is that trench formation has no etch-stop. Current etches for the fabrication of aluminum interconnects completely remove the primary metal or dielectric, and the process terminates on an etch-stop material (e.g., TiN). The within-wafer etch nonuniformity can thus be overcome by a modest over-etch. In the dual-damascene process, however, trenches are etched to an intermediate point part way through the dielectric layer. The within-wafer etch nonuniformity thus translates directly into within-wafer nonuniformity in the depth of the trenches.

A layered dielectric solves dual-damascene etch uniformity problems. The oxide dielectric is deposited in two separate layers - one for the line level and one for the via level - with a thin etch-stop material like silicon nitride deposited in between. Though this method provides a stop for the trench etch, it adds cost and complexity. It also increases the inter-level capacitance of the interconnect stack, which negates some of the gain in clock speed attained with lower-resistivity copper.

Challenges to the damascene etch process increase with each passing device generation. In order to maintain the lowest possible interlevel capacitance within the interconnect stack, it is desirable to shrink the width of vias and lines proportionately with the shrink in transistor gate length, while maintaining the largest practical spacing between metal levels [6]. Thus, each passing device generation has greater via aspect-ratios and an ever-increasing burden on the via etch and metal fill processes.

Copper fill

Metal fill by CVD is well known to chip manufacturers. Via fill by tungsten CVD is common in the fabrication of aluminum-based interconnects. As interconnects transition from aluminum to copper, CVD might also be the metal fill method of choice.

However, electroplating is an attractive alternative deposition method for copper that is not available for tungsten or aluminum. Electroplating is a very inexpensive process in principle, and a number of research groups have successfully used it to fill damascene structures [7]. A potential disadvantage of electroplating is that it is a two-step process. CVDfill can be completed in one step (directly on top of the diffusion-barrier), while electroplating requires deposition of a thin seed-layer prior to the plating fill step. The seed-layer provides a low-resistance conductor for the plating current that drives the process, and also facilitates film nucleation.

Although electroplating is a two-step process, calculations indicate that it offers a lower overall cost-of-ownership (COO) than full-fill CVD (Fig. 3). This calculation assumes that the required copper thickness is 1.0 ?m, which acknowledges that large-area pads must be filled along with the finer-pitch lines and vias on each metal level. The COO calculation includes factors such as the cost of the deposition equipment, fab space, labor, and consumables, but neglects factors related to device or process yield. Each cost component is computed on a per-wafer basis, with an assigned throughput of 50 wafers/hour for each process.

gif/03JacFig2.gif

Figure 3. Cost-of-ownership comparison for copper fill by CVD vs. copper fill by electroplating.

The COO calculations for seed-layer deposition, as well as the full-fill copper CVD process, are based on our direct experience with CVD copper, CVD tungsten, and PVD Ti/TiN. The COO calculation for electroplating is supported by input from semiconductor manufacturers with direct process experience. Calculations clearly favor the two-step electroplating process over the one-step CVD fill process. The cost difference is mainly due to the lower capital and chemical costs of the electroplating process. Most importantly, a well-tuned electroplating process can fill high-aspect-ratio structures (Figs. 4 and 5).

The results of this comparative COO calculation change dramatically if the copper thickness is reduced from the 1.0-?m value assumed in Fig. 3 because the CVD chemical cost scales directly with thickness. Based on a copper CVD precursor price of $1.00/gram, our COO model indicates that this crossover point occurs at a copper thickness on the order of 4000 ?. For applications where thinner copper may be required, such as the fill of single-damascene vias, copper CVD becomes an attractive alternative to electroplating.

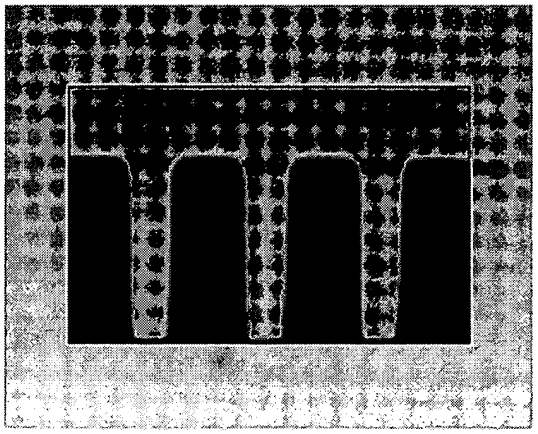


Figure 4. SEM cross-section of high-aspect-ratio trenches (0.28-?m wide, 5.0 aspect ratio) filled by electroplating. These trenches were plated over a tantalum barrier layer and a copper seed-layer, both deposited by PVD.

Copper contamination of the wafer bevel and backside is a significant concern for manufacturing. The most effective method to eliminate this source of contamination is to ensure that the wafer bevel and backside do not come in contact with the plating solution. Combining this method with a post-plating rinse can effectively eliminate copper contamination.

Since most semiconductor process engineers have little experience with electroplating, there tends to be a natural preference for more familiar copper-fill methods (i.e., CVD, or directional PVD and reflow). However, copper electroplating`s low cost creates a strong motivation for process engineers to examine it thoroughly. The process should gain acceptance.

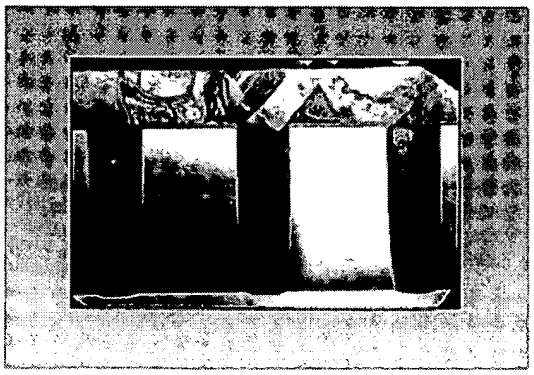


Figure 5. TEM cross-section showing high-aspect-ratio vias (0.35-?m wide, 3.4 aspect ratio) filled by electroplating. The vias were plated over a PVD tantalum barrier layer and a CVD copper seed layer.

Pre-clean, barrier and seed-layer deposition

The via pre-clean, barrier deposition, and seed-layer depositions will be combined on a vacuum-integrated

platform to ensure that low-resistance vias are fabricated with high yield. The pre-clean removes oxides and etch residues that contaminate the metal surface at the bottom of a via; it will initially use argon-ion sputtering. A dual-frequency RF sputtering module with an HDP source is required, so that a high level of directionality can be achieved in the sputtering process at high etch rates.

During pre-clean, copper ejected from the lower layer will be re-deposited onto the via sidewalls prior to deposition of a diffusion barrier, increasing the risk of line-to-line leakage. The magnitude of this problem is yet to be determined, though it is very likely that the quantity of copper re-deposited during preclean will be insufficient to degrade device performance. Otherwise, alternate via pre-clean methods will be required selectively to remove etch residue and copper oxides in the presence of copper metal.

The leading diffusion-barrier process and material is PVD of tantalum. Tantalum is an attractive barrier material because of its high melting point and its immiscibility with copper [8, 9]. It is also a highly reactive metal that forms strong metal-metal bonds, much like titanium (the standard contact layer for aluminum interconnects). Tantalum should thus provide a low-resistance Ohmic contact with excellent adhesion to copper. Doping the tantalum film with a few percent of nitrogen blocks grain boundary diffusion pathways. More heavily nitrided tantalum, produced by reactive sputtering of tantalum in the presence of nitrogen, is also a highly attractive barrier material [8, 9].

One specific advantage of PVD tantalum is the excellent step coverage achieved by the tantalum sputtering process (Fig. 6). The step coverage of PVD tantalum can be further extended by ionized PVD techniques, where a significant fraction of the atoms sputtered from the target material are ionized. Ionized PVD methods greatly enhance the step coverage of the PVD Ti/TiN deposition process [10].

At some future device generation, PVD techniques will probably not provide sufficient step coverage to deposit a diffusion barrier of the required thickness at all points within a high-aspect-ratio via. CVD diffusion barriers will then be required. The leading CVD barrier material for both copper and aluminum interconnects is TiN [11]. Alternative materials for CVD barrier layers include tungsten nitride and titanium silicon nitride.

In order to produce a uniform, adherent film of electroplated copper, a seed layer must be deposited over the barrier layer. The seed layer provides a low-resistance conduction path for the plating current that drives electroplating, and functions as a nucleation layer for copper film growth. Copper is the preferred seed layer because of its high conductivity, and because it is the ideal nucleation layer for growth of the electroplated copper.

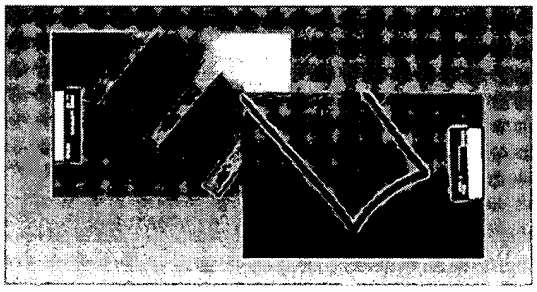


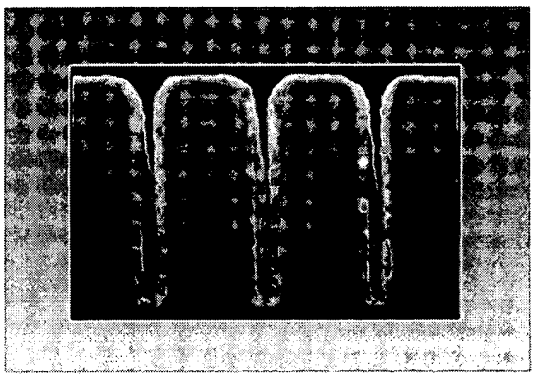
Figure 6. TEM cross-section showing the conformality of a tantalum layer deposited by PVD into a high-aspect-ratio trench (0.28-?m wide, 5.0 aspect ratio).

The copper seed layer plays two critical roles as a carrier of plating current. On the wafer scale, the seed layer carries current from the edge of the wafer to the center, allowing the plating current source to contact the wafer only near the edge. The thickness of the seed layer must be sufficient so that the voltage drop from wafer edge to center does not reduce the electroplating within-wafer uniformity. On a highly localized scale, the seed layer carries current from the top surface into the bottom of vias and trenches. When there is insufficient seed-layer thickness at the bottom, the via or trench will prematurely close during deposition, leaving a center void.

In principle, the seed-layer thickness at the bottom of a high-aspect

-ratio feature can be increased by increasing the thickness of copper deposited on the field. In practice, however, excessive seed material deposited at the field level will pinch off the via or trench, again creating a center void in the film.

Although PVD copper has limited step coverage in high-aspect-ratio vias and trenches, it has been successfully applied to electroplated fill. The trench structure shown in Fig. 4 was filled using a PVD tantalum barrier layer and a PVD copper seed layer. The PVD copper process for seed-layer deposition will be adequate for the first applications of copper, where the narrowest feature widths will be ~0.3 ?m. Beyond this, the PVD copper seed layer can be extended through ionized PVD methods. As with the barrier layer, however, a CVD seed layer will probably be required in future device generations.



SST/Marcia Jackson/Fig. 7

Figure 7. SEM cross-section showing the conformality of a copper layer deposited by CVD into a high-aspect-ratio trench (0.18-?m wide, 7.2 aspect ratio).

Copper CVD is attractive for seed-layer deposition primarily because it is capable of nearly 100% step coverage (Fig. 7). The 3.5:1-aspect-ratio via illustrated in Fig. 5 was filled using a CVD copper seed layer with copper electroplating. The superior step-coverage of the CVD copper process requires no additional cost relative to a PVD process; chemical costs that limit full-fill applications of CVD copper are greatly reduced because precursor usage is minimal for the very thin films required in a seed-layer application. Finally, the CVD copper seed-layer process can be extended to fill narrow vias completely in a single-damascene application, which will be a significant advantage in future device generations, where even a relatively thin seed layer could pinch off a very narrow via.

CMP

Copper is a readily oxidized, ductile material that is ideally suited to the CMP process. These properties translate into a very high copper removal rate, but they also contribute to dishing problems [12]. Dishing is defined as excessive removal of material in large surface-area pad features relative to smaller surface-area lines and plugs.

The tantalum diffusion barrier complicates copper CMP. Once the copper layer is completely polished back, the underlying tantalum layer must also be removed from the field level. The pad/slurry combination used for copper CMP does not effectively remove tantalum. Alternative pad/slurry combinations have been developed for CMP of tantalum, but the selectivity of these combinations for tantalum relative to copper has not yet been optimized. As a result, dishing is more difficult to eliminate when a tantalum barrier layer is used, because tantalum must be polished back in the presence of exposed copper damascene features. It is thus desirable to minimize the field-level thickness of the tantalum film. Titanium nitride does not have the same selectivity problem as tantalum, since pad/slurry combinations are available that can selectively remove TiN in the presence of copper.

The post-CMP clean step is a critical one for copper CMP. The bevel and backside of the wafer will most likely be exposed to copper-containing solutions during the CMP step. Any copper remaining on the bevel or backside of the wafer risks contamination of other tools within the fab. As in the electroplating process, simple cleaning methods are available to remove residual copper [13], but the risks associated with copper cross-

contamination demand careful monitoring of the post-CMP clean.

Conclusion

The basic process flow for copper damascene conductor fabrication is now well established, but significant challenges remain before copper processing becomes routine in manufacturing. Challenges include controlling the risks of copper cross-contamination within the fab, and the lack of familiarity among semiconductor process engineers with electroplating. In dual-damascene applications, additional challenges are presented by the via-etch process and the post-via-etch lithography step used to define the trenches.

Several additional issues must be addressed as copper interconnects extend to the 0.13-?m device generation and beyond: extendibility of via-etch to very high aspect ratios, step coverage of the barrier and seed layers, electroplated fill of extremely narrow vias, and integration with low-k dielectrics. The clock-speed and electromigration advantages of copper provide strong motivation to resolve all these challenges.

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